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THE AEROSPACE ENERGY SYSTEMS LABORATORY: HARDWARE AND SOFTWARE IMPLEMENTATION

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Abstract

For many years NASA Ames Research Center, Dryden Flight Research Facility has employed automation in the servicing of flight-critical aircraft batteries. Recently a major upgrade to Dryden's computerized Battery Systems Laboratory was initiated to incorporate distributed processing and a centralized database. The new facility, called the Aerospace Energy Systems Laboratory (AESL), is being mechanized with iAPX86 and iAPX286 hardware running iRMX86. This paper describes the hardware configuration and software structure for the AESL.

Nomenclature

A/D	analog-to-digital
ADC	analog-to-digital converter
AESL	Aerospace Energy Systems Laboratory
Ames-Dryden	NASA Ames Research Center, Dryden Flight Research Facility
BSC	Battery Station Controller
BSL	Battery Systems Laboratory
DAC	digital-to-analog converter
DPR	dual port RAM
DSDD	double-sided, double density
IEEE	Institute of Electrical and Electronic Engineers
I/O	input/output
NDP	numeric data processor
SBC	single-board computer
SBX	single-board expansion
SCP	status and control panel
TTL	transistor-transistor logic

Introduction

For many years the NASA Ames Research Center's Dryden Flight Research Facility (Ames-Dryden) has been operating research aircraft in which rechargeable batteries serve as important power sources for various flight-critical systems. Such batteries must undergo periodic servicing to verify integrity, capacity, and load-carrying ability for flight safety recertification. Because of the large number of aircraft, each having several sets of batteries assigned to it, the servicing workload is considerable. Ames-Dryden has been incorporating automation techniques to lower the cost of battery servicing, while at the same time improving quality and reducing turnaround times.

The present Ames-Dryden Battery Systems Laboratory (BSL) evolved over 20 years, based on goals established in the 1960s. In 1970 automation was first introduced into the BSL using a commercial minicomputer and a 200-channel scanner employing a multiplexed analog-to-digital converter (ADC). This system was so successful that in 1973 the minicomputer was upgraded and the ADC expanded to 800 channels. A modernization effort beginning in 1979 brought the system up to 1024 ADC channels, and a new computer system allowed control over 40 battery-charging stations (Stewart, 1983).

In 1987 it was decided that the BSL required further modernization to meet projected future requirements for battery servicing at Ames-Dryden. The second-generation BSL will be called the Aerospace Energy Systems Laboratory (AESL) (Glover, 1988b); prototype elements of this new system are nearing operational status. This report discusses the implementation of the new facility based on prior Multibus systems engineering done at Ames-Dryden to support aircraft testing (Glover, 1983; Glover, 1987; and Glover, 1988a).

Evolution of the AESL

Figure 1 is an overview of NASA's present Battery Systems Laboratory (BSL). The system employs a minicomputer and a centralized analog data acqui-

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sition system to receive 25 data channels from each of 40 battery servicing positions. Although not shown in figure 1, the minicomputer has shutdown command authority over the charger at each position. Servicing records are sent to the line printer and filed as hardcopy for later reference. A portion of this hardcopy listing is then manually entered into a separate servicing record archives for ease of access.

After many years of automated battery servicing, the BSL has reached the end of its useful service life. Hardware and software maintainability has diminished and the architecture has inherent single point failures. Several shortcomings have also been identified: the analog-to-digital (A/D) sample rate is too low, A/D calibration is difficult, it cannot sense battery temperature, and ampere-hours integration accuracy is low. Following a detailed study of the BSL and its operational deficiencies (Glover, 1988b), the following requirements for a new facility were defined:

Improve Reliability

- New state-of-the-art hardware
- Decentralized architecture to reduce wiring
- Industrial grade real-time operating system
- Fault-tolerant partitioned system philosophy
- Stand-alone operations of system components

Upgrade Central System

- Incorporate battery-specific servicing history archives
- Incorporate project-specific applications database
- Incorporate battery-type characterisics database
- Incorporate independently powered clock and calendar

Improve Safety

- Incorporate cell emissions detector
- Incorporate case temperature sensing
- Incorporate runaway cell detection algorithm
- Incorporate deadman timers in control loops
- Provide independent primary power shutdown relays

Improve Accuracy

- Increase data acquisition sample rate
- Perform amp-hour integration at 100 Hz or more
- Incorporate algorithms for pulsed waveform analysis
- Incorporate provisions for ADC calibration

Improve Productivity

- Provide technician I/O at each battery station
- Minimize technician keyboard operations
- Provide rapid battery identification by barcode tags
- Automate case leakage current measurement
- Permit unattended overnight and weekend operations

The new battery servicing facility will be called the Aerospace Energy Systems Laboratory (AESL). The AESL will employ distributed processing linked to the central system by way of a serial data cable, as shown in figure 2. The central system will not only serve as host for an integrated file structure, but will also serve as a data bus manager, a multiple-user timesharing interface, and a software production facility.

Figure 3 is an overview of an AESL battery station, and figure 4 shows how the station components are physically arranged. The charger is mounted on the top shelf and a status and control panel (SCP) is mounted near eye level at the front edge of the top shelf. The battery being serviced sits on the middle shelf with the monitor plate clamped to its top. The power relays are located in the large box visible at the rear of the middle shelf. The controller subsystem sits on a shelf immediately below the middle shelf, with the current shunt nearby (not visible). Not shown in the photo are the temperature probes, four of which are placed beneath the battery case, and a fifth probe inserts into the monitor plate. Also not shown is the load bank which is a separate piece of equipment used for variable-load profile testing.

Figure 5 shows a functional overview of the AESL. A typical battery servicing operation begins with the battery lab technician selecting a task on the SCP switch matrix. The technician identifies the battery

to be serviced by scanning its affixed barcode tag using the hand-held barcode reader gun attached to each battery station. He identifies himself as the servicing technician by scanning a personalized credit-card-sized barcode ID. The appropriate specification files are fetched from the central system, starting with the battery specification file using a path name constructed from the battery barcode tag; the remaining files are fetched using pathnames derived from information found in the battery specification file. The technician fastens the monitor plate and temperature probes to the battery, presses the EQUIP POWER button (which supplies power to the charger) on the SCP, adjusts the charger with the appropriate setting, and starts the servicing operation by selecting run mode on the SCP.

During the operation, the controller monitors all the variables and senses both normal end-of-run and out-of-limits conditions. At the completion of the operation, the station controller shuts down the charger by way of primary power relays external to the charger, alerts the technician with the sounding of the beeper alarm and display of an end of operation status message on the SCP, and transfers the data generated during the operation to the central system archives.

Database Specification and File Structure

One of the first elements to be designed for the proposed new facility was the integrated specifications database and battery servicing records archives file structure shown in figure 6. The root directory BATTERY will contain second-level battery directories with names corresponding to their eight-digit barcode numbers. Each of these second-level directories includes a single specification file and any number of data files created during battery servicing operations. The names of these data files will be generated from the date and time at the moment of file creation. Therefore, a file created at 8:30 a.m. on November 15, 1988 would be named 881115083000. Within the root directory CELL will reside the cell specification files, one for each type of cell used in the various types of batteries. The root directory PROJECT will contain second-level project directories. Each second-level project directory will contain a single project specification file and also may contain any number of variable-load profile files.

Management of this integrated data structure has several operational aspects. First, the structure must be expandable as new batteries, cell types, and projects are added. This requires creation of additional directories and editing of new specification files. Second, there must be utilities for decoding specification files and encoding servicing data files. Third, to permit efficient access to the servicing data files, there must be application utilities for scanning, cross-correlating, and extracting the desired information. Last, there must be an efficient means for culling older data files so they may be stored off-line.

Two alternate methods of structuring the specification and data files were considered: ASCII text files and a combination of ASCII and raw numeric. A portion of both the specification and data file contents was expected to be ASCII, while the remainder was mostly floating-point numeric. It was decided to design the entire structure using only ASCII-encoded text files. The disadvantage of this strategy is that the files are larger, while the advantage is ease of editing. The format chosen was free-field using parameter identification tags and field delimiters as opposed to fixed-length fields, thus offering maximum flexibility. Figure 7 shows an example of a cell specification file illustrating the type of parameters and characteristics included. Figure 8 shows an example of a battery servicing data file.

Central System Mechanization

As shown in figure 9, the AESL central system consists of a two-chassis Intel System 310 processor on the left, a Wyse Model 60 terminal in the center, and a Dataproducts M220 line printer on the right. The 310 main subsystem chassis mounted on top has installed a Memtech iBC magnetic bubble cassette module, a 5.25-in. DSDD floppy diskette drive, and a 0.25-in. tape cartridge drive. The 311 peripheral expansion subsystem chassis on the bottom has installed two Seagate ST251 hard disk drives and associated power supplies.

Table 1 shows the hardware complement installed in the 310 cardcage. The processor is an SBC 286/12 that has an 80287 numeric data coprocessor installed, plus a SBX344A BITBUS interface module installed at SBX connector J6. The SBC544 and SBC548 communications controllers provide a total of 12 channels of serial I/O. The SBC214 provides management of the hard disks, the floppy drive, and the tape drive. The Central Data motherboard hosts an assortment of supporting SBX modules. The SBX258 module interfaces to the iBC bubble cassette unit. The SBX351 serial module provides a utility RS232 port.

The SBX251 magnetic bubble memory module provides 128 Kbytes of auxiliary scratchpad. The Computer Modules LSBX-Super module is powered by a lithium battery and provides clock/calendar services, a programmable timer interrupt, and 8 Kbytes of nonvolatile static RAM.

The operating system used in the AESL central system is RMX86 Release 7 containing a full complement of system services including Universal Development Interface (UDI). The program is configured for the peripherals described above using the interrupt mapping shown in figure 10. The iBC bubble cassette unit is configured as unit :B0: and the SBX251 auxiliary bubble memory is configured as unit :B1:. The hard drives are configured as units :W0: and :W1:, with :W0: serving as the system device and :W1: serving as the repository for the integrated database structure. For both the central system applications and BSC software :W0: is formatted for 5000 files and hosts the software production tools and miscellaneous source language elements. On the assumption that virtually all its files will be less than 1024 bytes in length, :W1: is formatted for 38,000 files. No software is yet in place to service either the multiuser environment or the BITBUS, and the central system has thus far only been used for the production of BSC software.

Battery Station Controller Mechanization

As shown in figure 11, the BSC consists of an SBC 661 chassis modified with a housing for a pair of iBC cassette bubble memory units (labelled PROGRAM and DATA) on top of the chassis and an auxiliary power connector box at the right side. Additional internal modifications include an AC low interrupt and a 120-Hz clock interrupt. The front cover has been machined with mounting holes for the ribbon connector assemblies which provide I/O interfaces to the cardcage. Figure 12 shows an overview of the major components of the BSC.

Table 2 shows the hardware complement within the SBC 661 cardcage, and figure 13 shows the installed components. The processor is an SBC 86/35 with an 8087 numeric data coprocessor installed. Both its SBX connectors are occupied: J3 contains a General Digital GDX-Proto-1 board used to interface to the SCP display, and J4 contains a SBX344A BITBUS interface module. The Central Data motherboard hosts an assortment of supporting SBX modules. The SBX351 serial module provides a utility RS232 port. The General Digital GDX-Barcode module provides the interface to the hand-held barcode reader gun. The SBX258 module interfaces to the two iBC bubble cassette units. The Computer Modules LSBX-Super module is identical to that installed in the central system providing clock/calendar, timer, and nonvolatile RAM. The Datel ST-701-A2 and ST-742 boards comprise the 48-channel analog input subsystem. The Analog Devices RTI-724V board provides four channels of analog output. The Burr-Brown MP830-72 board provides miscellaneous transistor-transistor logic (TTL) discretes for servicing the SCP.

The operating system used in the BSC is RMX86 Release 7 but contains only the full nucleus and full basic I/O. The program is configured for the peripherals previously described using the interrupt mapping shown in figure 14. The iBC PROGRAM bubble cassette unit is configured as :B0: and is the boot device. The iBC DATA bubble cassette unit is configured as :B1: and contains a file structure identical to the central system integrated database.

Figure 15 shows the mapping of the BSC software and hardware. The SBC 86/35 board is configured for the maximum EPROM complement of four 27256s. These PROMs contain the bootstrap loader, an SDM monitor, the RMX86 nucleus, and the RMX86 basic I/O. The DAC board occupies an 8-byte slice starting at 0DAC00H, and the A/D subsystem occupies 8 Kbytes starting at 80000H. The lower 512 Kbytes of memory address space is occupied by the RAM on the SBC 86/35 board. This is divided equally between the user job (upper half) and RMX86 (lower half). The file /SYSTEM/RMX86 found on :B0: consists of the ROOT job (mapped at 01100H) and the user job (mapped at 40000H).

During the preliminary design of the BSC user job, it was decided not to use RMX86 segments for shared data areas. Instead, shared elements were simply declared PUBLIC using PLM86 LARGE model such that all tasks could access all elements. This eliminated all catalog entries and searches, simplified initialization, and reduced the size of the user job by several percent.

The BSC user job consists of a mix of PLM86 and ASM86 modules. Table 3 lists the task complement within the BSC user job. The total number of tasks is 23, and resource allocation is performed using regions. The following hardware regions are employed: CRT, B0, B1, LSBX, NDP, ANALOG, DISPLAY, and PRINTER. A software region, STATUS, is used to

avoid conflicts in updating and accessing the PUBLIC variables defining the operational status of the BSC. All regions are created using task priority queueing.

A total of 11 semaphores are employed within the BSC user job. Seven of these are configured as SIGNAL$PAIR semaphores providing keyboard traps for special function keys. A task is associated with each to set the corresponding PUBLIC flag to true. The remaining four semaphores are used for intertask synchronization. While all semaphores are configured for first-in first-out queueing, only a single task waits at each.

One special interrupt handler is employed to intercept the nonmaskable interrupt (NMI) interrupt linked to the AC low signal generated by the BSC power supply. This handler sets a four-byte power fail flag in the LSBX RAM and halts the processor. Whenever the BSC is powered up, this flag is checked; if set, a special power fail recovery routine is invoked.

Figure 16 shows the mechanization of the leakage relays control interface. Bits 0 and 4 of the SBC 86/35 status register are used to control the positive and negative pole relays, respectively. Battery leakage-case-to-positive is measured by momentarily connecting a 50-ohm resistor between the case and the positive pole of the battery then measuring the voltage across the resistor. The process is repeated for the negative pole. The LEAKAGE task wakes up every 15 sec and exercises both relays through transistor switches, taking autoranging readings of the resistor voltage and computing the currents.

Figure 17 shows the mechanization of the power relay control interface. Status register bit 1 is used to gate timer 1 of the 8253 programmable interval timer chip. Timer 1 is set up as a programmable one-shot multivibrator (mode 1) and is loaded with a maximum of 65,535 counts, giving a pulse width of 420 msec. The EQUIP$POWER task wakes up every 250 msec and toggles the gate to keep the timer 1 output low and, hence, keep the power relays closed. Should either hardware failure or software deadlock prevent it from doing so, timer 1 opens the relays.

Analog Subsystem Mechanization

Figure 18 shows a simplified block diagram of the A/D subsystem utilized in the BSC controller. The subsystem consists of two boards: a DATEL ST-701-A2 16-channel intelligent A/D board and a DATEL ST-742 32-channel expander. The ST-701 board contains a 4-MHz Zilog Z-80A microprocessor, an 8 K PROM, an 8 K local RAM, and a 4 K static dual-port RAM (DPR). The programmable gain amplifier (PGA) offers gain steps from X1 to X128. The SBC 86/35 control and data interface to the ST-701 is through the DPR using 8-bit and 16-bit operations.

Table 4 lists the A/D channel assignments. Channel addresses 0 through 15 select analog inputs locally multiplexed on the ST-701 board. Channels 16 through 47 are located on the ST-742 expansion board.

In order to streamline the A/D subsystem operation, the factory-supplied firmware was removed and a NASA-designed program consisting of a mix of PLM80 and ASM80 modules was substituted. It provides semiautonomous operation of the ST-701 in several different modes through an algorithm selection routine. Control of the ST-701 is accomplished through control flags mapped into the top of the DPR. The mapping of these flags and various data areas is shown in Table 5. The factory-supplied EPROM is retained and is used during off-line subsystem calibration.

The current waveform of the charger is a function of both the equipment type (charger) and the servicing task selected by the technician. The equipment type is made known to the program by fetching a 19-byte structure from the LSBX module RAM. This permanently stored array only needs to be changed by the technician when the charger is replaced with a different type. The task to be performed is selected by the technician using the SCP pushbutton matrix. The program then selects one of three algorithms: sample, burst, or scan, depending on which is appropriate for the waveform. Each time the charger is powered up, the program commands the ST-701 to do a hardware reset and then commands it to execute the selected algorithm.

The sample algorithm is the simplest of the ST-701 modes and is used only in the open circuit task when the waveform is direct current. In this mode, the ST-701 services all channels round robin and places the 16-bit integer A/D values in the latest sample array. The BSC program then asynchronously fetches the data it needs from this array. It takes typically 2 msec to complete a wraparound of the latest sample array. No ampere-hour integration is performed in the sample mode.

The burst algorithm is used when the current waveform contains only line frequency harmonics superimposed on direct current. In this mode, the ST-701 ser-

vices each channel in turn using a 1/60-sec window over which it takes as many samples as possible. An 8-bit tally is made of the number of samples taken (usually around 175) and each sample is added to a 24-bit signed sum. The resulting 32-bit "burst" is placed in a burst structure consisting of 16 arrays of 48 such 32-bit bursts. The last frame byte indicates which is the most recently updated array. The BSC program fetches the data it needs from the appropriate portion of the burst structure, and divides each 24-bit sum by its 8-bit tally to obtain the average value for a particular channel over the 1/60-sec window. It takes typically 800 msec to fill one array in the burst structure.

The scan algorithm is used for pulsed waveforms that contain frequencies lower than line frequency. The reflex charger waveform shown in figure 19 is one example of such a waveform. The setpoint for the charge operation is the plateau of the pulse; it is here that we wish to snapshot battery current and voltages. The scan algorithm makes this possible by providing 32 successive frames of input data, each of which consists of a sample array such as that generated by the sample algorithm. The last frame byte indicates which is the most recently filled array in the structure, and the ST-701 then sends an interrupt to the SBC 86/35. The BSC program monitors battery current at each interrupt and senses the descending node crossing a threshold equal to 50 precent of the setpoint current. The program then backs up five frames onto the plateau and averages the preceding 16 frames. The frames occur at typically 4 msec intervals, hence, the averaging window is approximately 64 msec.

Ampere-hour integration of battery current (channel 0) is performed in both burst and scan modes. The ST-701 performs the integration of battery current into a 64-bit sum while keeping track of the number of samples in a 64-bit tally counter. The BSC program sets the integral flag to obtain a snapshot of these two quantities and computes ampere-hours using elapsed time since ST-701 reset.

The measurement of leakage current employs an autoranging routine in the BSC program that interfaces to the single channel flags in the DPR. Every 15 sec, the leakage current task wakes up and in turn checks both the positive and negative poles of the battery. One of the two relays is turned on, a 30-msec wait occurs while the relay contacts close, the single channel flag is set to channel 42, the single channel gain is set to X1, and the single channel request flag is set to true. The ST-701 polls the single channel request flag at intervals that vary according to the algorithm, and clears the flag when the value has been placed in the latest sample array. The task steps the gain until the latest sample array shows a channel-42 value of > 30 percent of full scale or until gain X128 is reached. The entire process is repeated for the other relay.

Included in the AESL BSC main command menu is a schedule editor utility that enables the technician to control the timing and frequency of data file creation for each of the twelve battery servicing operations. The technician modifies the schedule to create files at the beginning of the run, end of run, or both, as well as at desired intervals throughout run.

A majority of the LSBX module's RAM is mapped into twelve 672-bit status-save buffers. When in run mode, a status snapshot is saved once/sec in one of these twelve buffers. A power-fail flag is set at the time of power failure, which at power up initiates a BSC power fail routine to, among other things, fetch the most recent status-save snapshot. A utility on the AESL BSC main command menu called "scratch" takes advantage of the existence of these status-save buffers by making available for display the 12-sec complement. Scratch allows the technician, when in open circuit, to step back through the scatch pad one status file at a time.

Implementation Status

The AESL Central System has been operational as a software production facility since November 1987. The :W1: hard disk has been formatted with a directory for 38,000 files. The integrated database tree structure is in place, and specification and data file formats have been finalized.

A prototype battery station has been constructed and final wiring harnesses are being engineered. The unit has been operating in stand-alone mode since May 1988 and the BSC software is undergoing verification and validation (V/V) testing. The A/D subsystem firmware has been evolving as changes are introduced to optimize interprocessor communications and increase sample rates. The latest change to the A/D firmware was the introduction of the "burst" algorithm to provide improved averaging for waveforms with large amounts of line frequency harmonics. This change proved very successful.

Considerable operational experience has been gained using the iBC bubble cassette subsystem and it has proved to be a highly reliable medium. BSC

program updates and specification files have been routinely ported from the central system to the prototype battery station. Confidence in this form of file management has permitted a range of operations scenarios to emerge. The original concept of data transfers on the BITBUS will be used whenever a battery station is connected to the bus, but the range of options in stand-alone mode has widened. Stand-alone operation of a battery station might occur if, for example, an aircraft is deployed to another flight test facility and a battery station is deployed with it, or a battery station might be temporarily relocated to the hangar to be closer to the aircraft. Such deployments require that the battery station be supplied with the requisite bubble cassettes having the needed specification files. One option is assigning a bubble cassette to a battery such that all of its related files (up to a maximum of 200) are on one device. The cassettes could be hand carried to the central system and the data files dumped to :W1: whenever desired. Another option is the dumping of files using a phone line modem link through the central system multiuser interface.

Following BSC program V/V, the prototype battery station will be turned over to BSL personnel for a 30-day shakedown in stand-alone mode. Special emphasis will be given to testing the technician interface routines and to the charger waveform analysis algorithms. Attention will then turn to development of the BITBUS software interfaces in both the central system and the BSC. Engineering changes to the SBX 344A are being considered to increase the message length as much as possible to speed file transfers. Considerable software engineering effort is anticipated to develop the BITBUS manager user job in the central system. Following this, the multiuser environment will be activated and database access utilities will be developed.

It is expected that sometime during CY88 the final approval will be given for the fabrication of a set of production battery stations. The presently planned initial configuration of the AESL is for a complement of 10 battery stations, all operating on the data bus. The prototype battery station unit will become an engineering brassboard used to evaluate new software and support research tasks investigating new techniques in battery servicing. Longer range plans for the AESL include eventually upgrading the central system to RMX286 with the addition of 4 Mbytes of RAM and replacement of the SBC 544 communications controller with either a SBC 544A or a second SBC 548. This enhancement will provide a better environment for the anticipated intensive multiuser operations.

Concluding Remarks

For many years the existing NASA Ames Research Center's Dryden Flight Research Facility automated Battery Systems Laboratory has provided a wealth of operations experience in the servicing of aircraft batteries. It will soon be replaced by the new Aerospace Energy Systems Laboratory that will provide a modernized facility containing numerous enhancements while retaining proven features. The new facility is now under development and its implementation builds on proven Multibus systems design experience gained from other programs at Ames-Dryden. Engineering prototype hardware has reached the testing stage, and early results indicate that the chosen implementation will meet the design requirements.

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TABLE 1. CENTRAL SYSTEM BOARD COMPLEMENT

310 Slot number	Installed Components
J7	CD21/6600 SBX motherboard (Central Data)
	Pos. 1 : SBX 258 iBC magnetic bubble interface
	Pos. 2 : empty
	Pos. 3 : SBX 351 serial I/O
	Pos. 4 : SBX 251 magnetic bubble memory (128K)
	Pos. 5 : empty
	Pos. 6 : LSBX-Super clock/calendar/RAM (Computer Modules)
J6	SBC 214 peripheral controller
J5	SBC 544 communications controller
J4	SBC 548 communications controller
J3	empty
J2	empty
J1	SBC 286/12 processor
	J5 : empty
	J6 : SBX 344A BITBUS interface

TABLE 2. BATTERY STATION CONTROLLER BOARD COMPLEMENT

661 Slot number	Installed Components
J1	CD21/6600 SBX motherboard (Central Data)
	Pos. 1 : empty
	Pos. 2 : SBX 351 serial I/O
	Pos. 3 : GDX-barcode interface (General Digital)
	Pos. 4 : SBX 258 iBC magnetic bubble interface
	Pos. 5 : LSBX-Super clock/calendar/RAM (Computer Modules)
	Pos. 6 : empty
J2	SBC 86/35 processor
	J3 : GDX-Proto-1 display interface
	J4 : SBX 344A BITBUS interface
J3	ST-701-A2 analog input processor (Datel)
J4	ST-742 analog input expander (Datel)
J5	empty
J6	empty
J7	RTI-724V digital-to-analog output (Analog Devices)
J8	MP830-72 TTL discretes I/O (Burr-Brown)

TABLE 3. BSC TASK ROSTER

Task name	Priority	Notes
MULTIPLEXER$TASK	019	Scans SCP pushbuttons & LEDs
ANALOG$TASK	020	Interrupt level 0010h
BARCODE$TASK	024	Interrupt level 0012h
LSBX$TASK	030	Interrupt level 0015h
EQUIPMENT$POWER$TASK	048	Controls power relays
BEEPER$TASK	050	Controls SCP beeper
BITBUS$TASK	066	Interrupt level 0038h
BSCJOB	132	User job
BSC$INIT$TASK	150	Created by BSCJOB
ESCAPE$TASK	155	Sets ESCAPE flag
HOME$TASK	155	Sets HOME flag
UP$TASK	155	Sets UP flag
DOWN$TASK	155	Sets DOWN flag
TAB$TASK	155	Sets TAB flag
TEMP$PROBES$TASK	201	Reads temperature probes
LEAKAGE$TASK	202	Measures battery case leakage current
SYNCH$TASK	210	Synchronizes data acquisition & display
MASTER$DISPLAY$TASK	220	Controls SCP display
PRINTER$POLL$TASK	225	Samples printer on-line status
PRINTER$TASK	230	Controls printer hardcopy (cntl P)
SUPERVISOR$TASK	240	Controls operation sequencing
DISPLAY$MODE$TASK	245	Samples display select pushbuttons
CRT$MENU$TASK	250	Manages terminal interfaces

TABLE 4. ANALOG TO DIGITAL CONVERTER CHANNEL ASSIGNMENTS

Channel	Assignment	Channel	Assignment
00	Charger amps	24	Cell 14 volts
01	Load bank amps	25	Cell 15 volts
02	Load bank volts	26	Cell 16 volts
03	Load bank deg	27	Cell 17 volts
04	Spare	28	Cell 18 volts
05	Spare	29	Cell 19 volts
06	Spare	30	Cell 20 volts
07	Spare	31	Cell 21 volts
08	Spare	32	Cell 22 volts
09	Spare	33	Cell 23 volts
10	Spare	34	Cell 24 volts
11	Cell 01 volts	35	Cell 25 volts
12	Cell 02 volts	36	Cell 26 volts
13	Cell 03 volts	37	Cell 27 volts
14	Cell 04 volts	38	Cell 28 volts
15	Cell 05 volts	39	Cell 29 volts
16	Cell 06 volts	40	Cell 30 volts
17	Cell 07 volts	41	Battery volts
18	Cell 08 volts	42	Leakage milliamps
19	Cell 09 volts	43	Top temp
20	Cell 10 volts	44	Case temp #1
21	Cell 11 volts	45	Case temp #2
22	Cell 12 volts	46	Case temp #3
23	Cell 13 volts	47	Case temp #4

TABLE 5. ST-701 DUAL-PORT RAM MAPPING

Address	Function
8FFFH	Interrupt doorbell
8F0FH	Run mode talkback
8F0EH	Run mode command
8F0CH	Single channel request
8F0BH	Single channel gain
8F0AH	Single channel number
8F04H	120-Hz clock flag
8F03H	Integral fetch flag
8F01H	Last frame number
8F00H	Algorithm number
8EF8H-8EFFH	Integral sum (64-bit long integer)
8EF0H-8EF7H	Integral number iterations (64-bit counter)
8E90H-8EEFH	Latest value array (48 integers)
8000H-8E8FH	Data output structures area (alternate overlays)

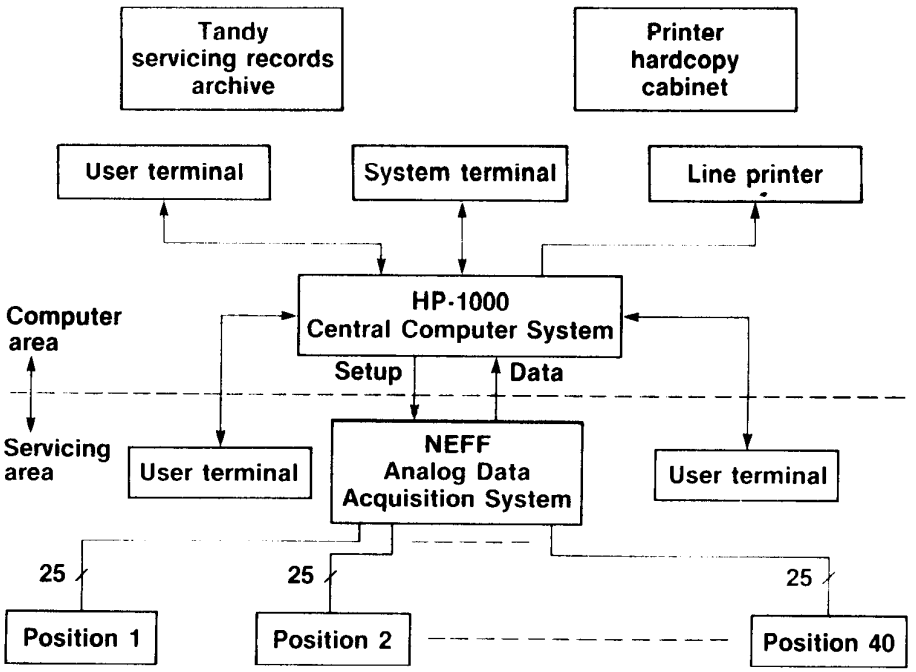


Fig. 1 Battery Systems Laboratory overview.

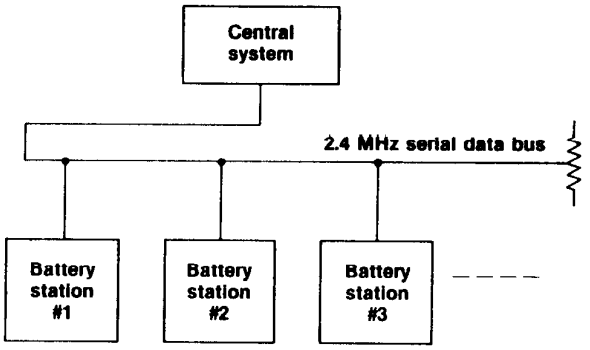


Fig. 2 AESL overview.

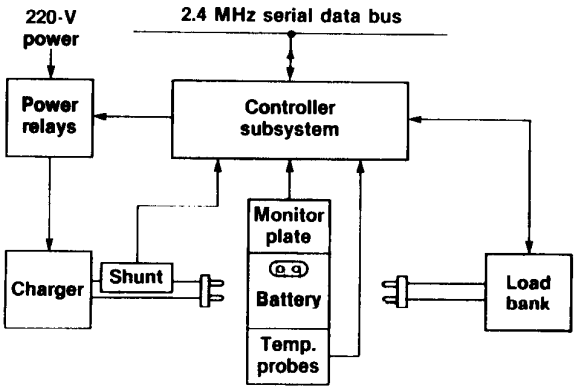


Fig. 3 AESL battery station overview.

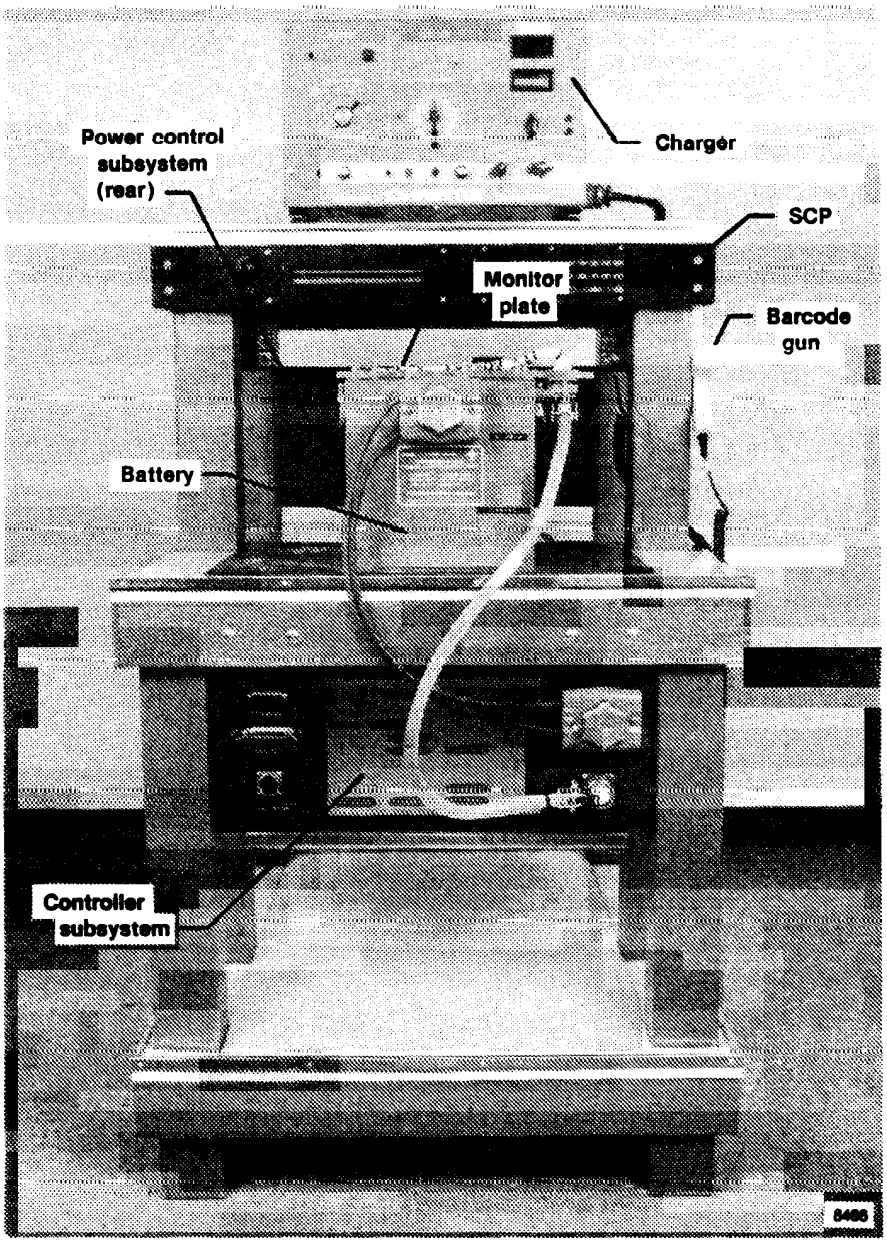


Fig. 4 Battery station bench.

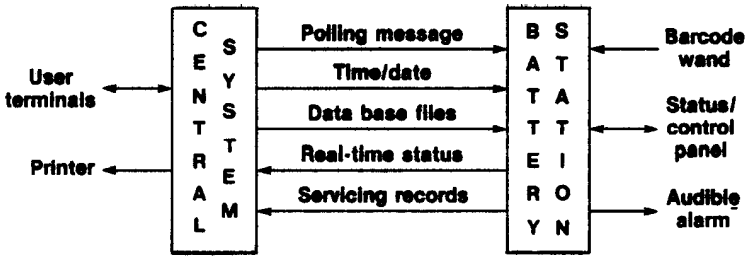


Fig. 5 AESL functional overview.

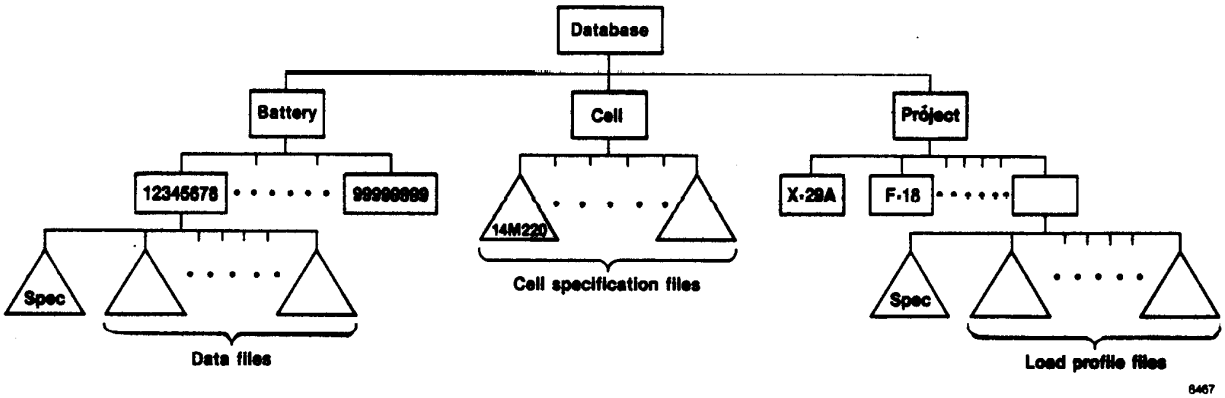


Fig. 6 Integrated database tree structure.

```
FILE=CSPEC;     CSPEC=14M220;   CTYPE=NiCd;     AHRATED=10.0;    MXAH=14
MXCHGV=1.75;    MXDIFFV=0.25;   MXDRGPV=0.03;   MXCHGT=115;
SETRFLI=14.0;   ENDRFLP=1.0;
SETPULI=14.0;
SET2MCI=10.0;   SET2TCI=5.0;    SET10CI=2.5;    ENDCIV=1.59;
SETCVV=1.70;    SETCVI=10.0;    ENDCVI=0.10;
VENTPSI=2.0 to 10.0;            CASEPSI=10.0;   TORQUE=20.0;
                                                                8481
```

Fig. 7 Example cell specification file.

```
FILE=BATTDATA;  BATTDATA=880817140007;  BATTSPEC=12345678;  STATION=27;
TASK=Capacity Test;  OPERATOR=Dan Smith;
PROJECT=TEST;  MODELNO=CA-5-20;  AHRATED=30.0;  NUMCELLS=20;
EQUIP=Christie Reflex;  STATUS=End of run;  PERIOD=;
BATTVOLTS=22.193;  BATTAMPS=-29.685;  ELAPTIME=01:20:48;  AH=-38.129;
TEMPS=91.281,98.896,94.251,96.788,96.365;
LEAKAGE=0.495,-0.404;
CELLVOLTS=1.14,1.13,1.12,1.11,1.15,1.09,1.09,1.12,1.09,1.12,1.12,1.13,
1.10,1.13,1.13,1.10,1.14,0.99,1.10,1.08;
CAUTWARN=Cell 18 minimum volts;
                                                                8480
```

Fig. 8 Example battery servicing data file.

EC88 0168-003

Fig. 9 Central system console.

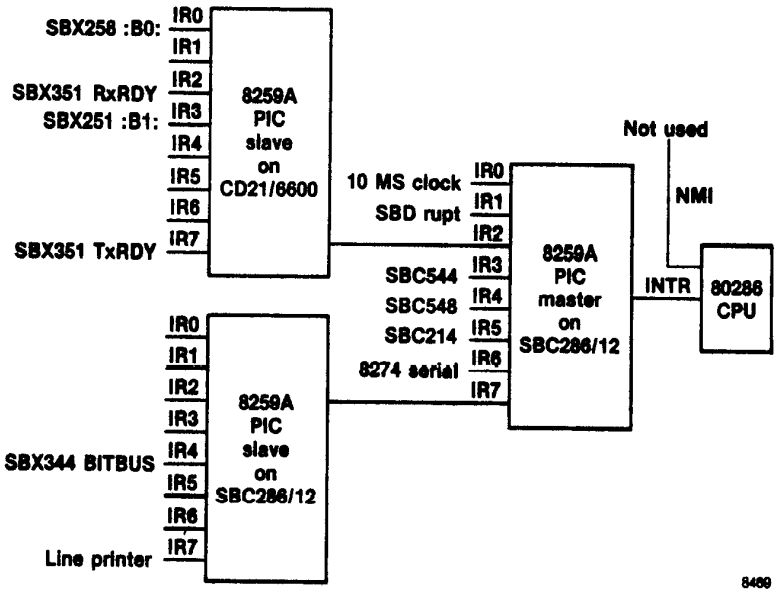
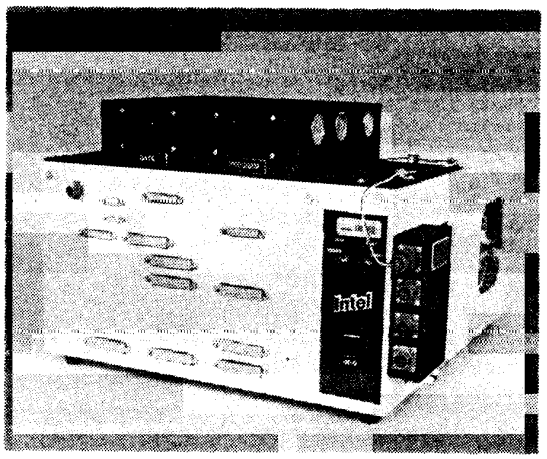


Fig. 10 Central system interrupt configuration.



EC88 0168-002

Fig. 11 Battery station controller subsystem chassis.

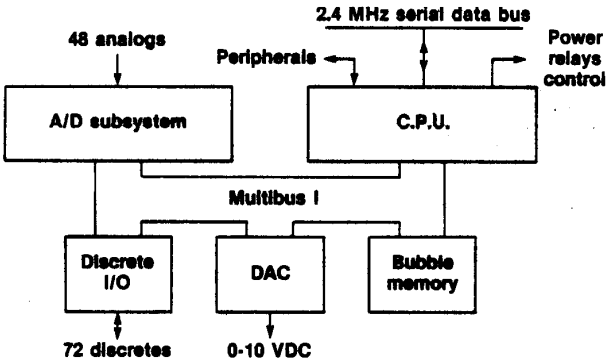
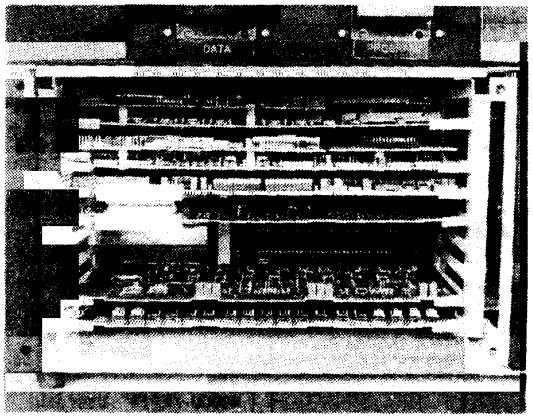


Fig. 12 BSC overview.



EC88 0168-004

Fig. 13 BSC cardcage.

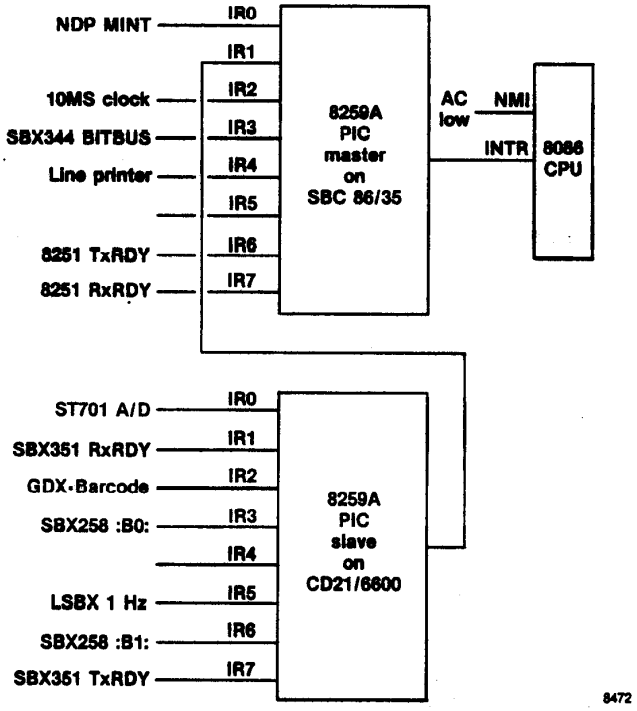


Fig. 14 BSC interrupt configuration.

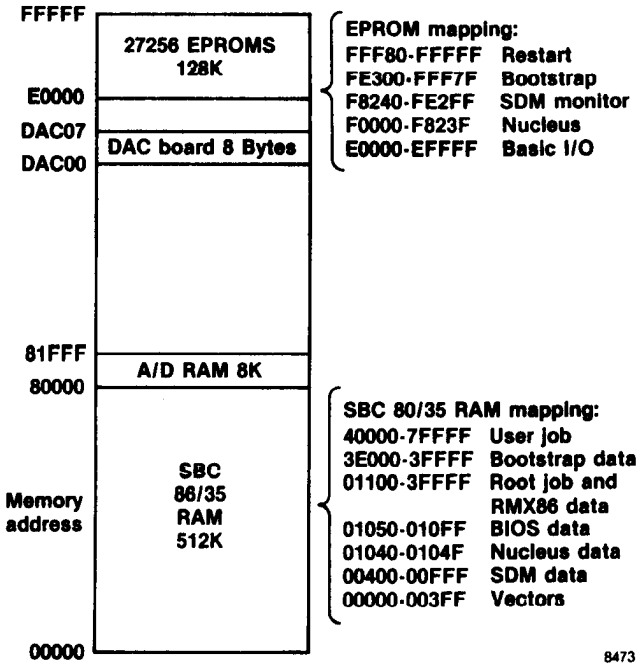


Fig. 15 BSC memory mapping.

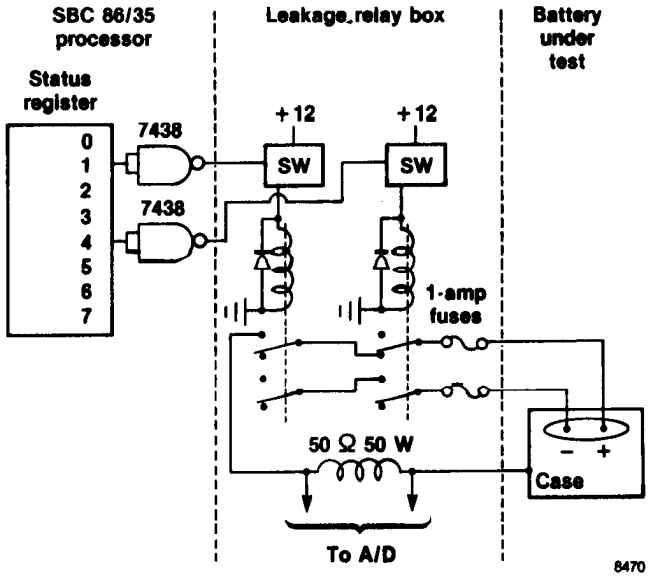


Fig. 16 Leakage relays control.

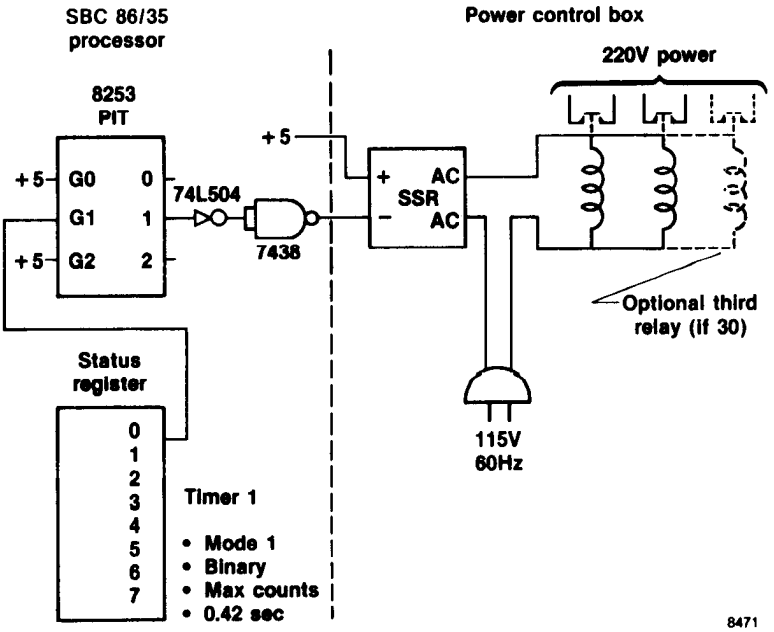


Fig. 17 Power relay control interface.

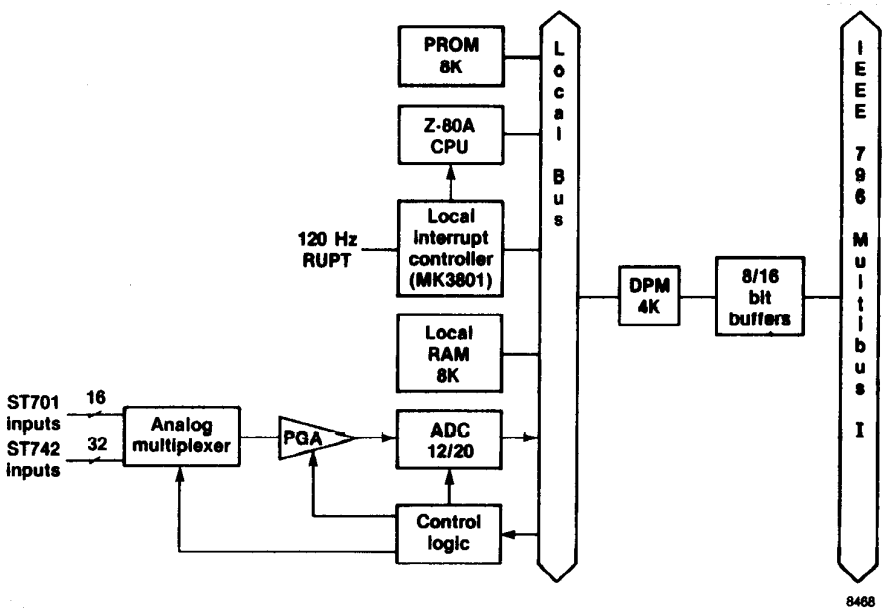


Fig. 18 AESL BSC analog subsystem overview.

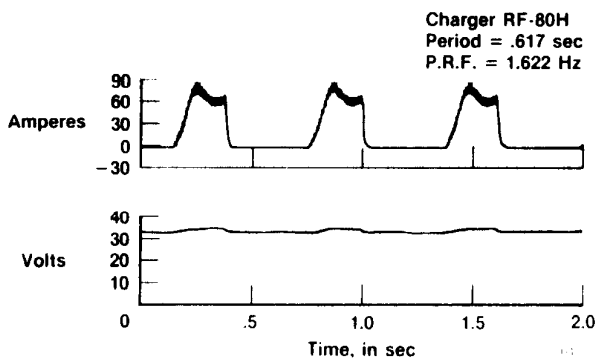


Fig. 19 Reflex charging waveforms.

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15. Supplementary Notes

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16. Abstract

For many years NASA Ames Research Center, Dryden Flight Research Facility has employed automation in the servicing of flight-critical aircraft batteries. Recently a major upgrade to Dryden's computerized Battery Systems Laboratory was initiated to incorporate distributed processing and a centralized database. The new facility, called the Aerospace Energy Systems Laboratory (AESL), is being mechanized with iAPX86 and iAPX286 hardware running iRMX86. This paper describes the hardware configuration and software structure for the AESL.

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